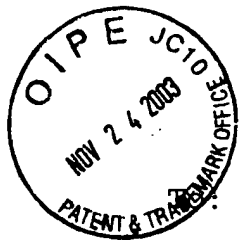


TSMC-01-999



November 18, 2003

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/650,601 08/28/03

Shih-Chi Lin

METHOD OF MANUFACTURING DIELECTRIC
ISOLATED SILICON STRUCTURE

Grp. Art Unit:

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.


The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on November 21, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 11/21/03

TSMC-01-999

U.S. Patent 5,091,330 to Cambou et al., "Method of Fabricating a Dielectric Isolated Area," describes a method of fabricating a dielectric isolated area.

U.S. Patent 5,466,631 to Ichikawa et al., "Method for Producing Semiconductor Articles," describes a method for producing a semiconductor article.

U.S. Patent 5,773,352 to Hamajima, "Fabrication Process of Bonded Total Dielectric Isolation Substrate," describes a fabrication process of bonded total dielectric isolation substrate.

U.S. Patent 5,950,094 to Lin et al., "Method for Fabricating Fully Dielectric Isolated Silicon (FDIS)," describes a method for fabricating dielectric isolated silicon.

Sincerely,

A handwritten signature in black ink, appearing to be 'SBA', written over a horizontal line.

Stephen B. Ackerman,
Reg. No. 37761

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.